What is claimed is:

1. A method of determining a frequency at which a terminal transmits a transmission signal, said terminal comprising a receiver including a delay lock loop circuit, the method comprising:

receiving an input signal at said receiver;

sampling said signal at a clock rate to generate signal samples;

providing said signal samples to said delay lock loop circuit;

controlling said delay lock loop circuit to provide an output representing a phase delay of the received signal;

adjusting the clock rate based on said phase delay; and

determining said frequency at which said terminal transmits said transmission signal based on said phase delay.

2. The method of claim 1, wherein said input signal comprises synchronization information in discontinuous time slots.

3. The method of claim 1, wherein said delay lock loop circuit comprises at least a third order loop.

4. The method of claim 3, wherein:

said delay lock loop circuit further comprises a low order gain loop; and

said step of controlling said delay lock loop circuit further comprises initially using said low order gain loop and subsequently using said at least third order loop to provide said output.

5. The method of claim 4, further comprising:

determining a difference between said frequency and an expected frequency; and

wherein the step of controlling said delay lock loop further comprises using said low order gain loop until said difference is less than a threshold value, and subsequently using said at least third order loop.

09768728.012401

6. The method of claim 4 wherein said controlling step uses said low order gain loop for a set period of time.

7. A method of determining whether a receiver of a satellite terminal is locked onto an incoming communications signal, the signal comprising a plurality of frames each having one out of a series of unique phase signals time division multiplexed into at least one time slot of the frame, the plurality of frames forming a superframe, such that the series of unique phase signals repeats in each subsequent superframe, the method comprising:

generating local phase signals substantially identical to the series of phase signals in the incoming signal;

delivering a combination signal representing a combination of the incoming signal and the local phase signals to a fast Fourier transform (FFT) circuit, the FFT circuit generating an output based on said combination signal;

determining whether the satellite terminal is locked onto the incoming signal based on the output of the FFT circuit.

8. The method of claim 7, wherein said local phase signals comprise a series of digital values.

9. The method of claim 7, wherein the incoming signal comprises a series of digital samples generated at a sampling rate.

10. The method of claim 9, further including the steps of determining an offset between the frequency of the incoming signal and the sampling rate based on the output of the FFT circuit, and adjusting the sampling rate based on said offset.

11. The method of claim 7, wherein the delivering step includes multiplying said incoming signal and said local phase signals to generate a product signal.

12. The method of claim 11, wherein the delivering step includes decimating said product signal to create said combination signal.

13. A system for tracking a frequency at which a transmitter transmits a signal, said signal comprising synchronization information in discontinuous time slots, said system comprising:

a receiver for receiving said signal,

a local signal generator for generating an early local signal and a late local signal at a local frequency, said early local signal being substantially similar to said synchronization information offset forward in time, said late local signal being substantially similar to said synchronization information offset backward in time,

a discriminator for correlating said signal against said early local signal and for correlating said signal against said late local signal, and for generating a discriminator output representative of the difference between the two correlations, and

a delay lock loop circuit for receiving said discriminator output, wherein said delay lock loop circuit generates an output which is used to adjust said local frequency.

14. The system of claim 13 wherein said delay lock loop circuit comprises at least a third order tracking loop.

15. The system of claim 14, wherein:

said delay lock loop circuit further comprises a low order gain loop; and

said delay lock loop circuit initially uses said low order gain loop and subsequently uses said at least third order tracking loop to provide said output.

16. The system of claim 15, further comprising:

a frequency offset determining circuit adapted to determine a difference between the frequency of said signal and an expected frequency; and

wherein said delay lock loop circuit uses said simple gain loop until said difference is less than a threshold value.

17. The system of claim 15, wherein said delay lock loop circuit uses said low order gain loop for a set period of time.

18. A system for determining whether a receiver of a satellite terminal is locked onto an incoming communications signal, the signal comprising a plurality of frames each having one out of a series of unique phase signals time division multiplexed into at least one time slot of the frame, the plurality of frames forming a superframe, such that the series of unique phase signals repeats in each subsequent superframe, the system comprising:

a sampling circuit adapted to sample the incoming communication signal at a sampling rate and for producing a series of samples at the sampling rate;

a local signal generator adapted to generate local phase signals substantially identical to the series of unique phase signals in the incoming signal at the sampling rate;

a fast Fourier transform (FFT) circuit adapted to receive a combination signal representing a combination of the samples and the local phase signals; and

a lock detector adapted to determine whether the satellite terminal is locked onto the incoming communication signal based on the output of the FFT circuit.

19. The system of claim 18, further comprising an offset estimator adapted to determining an offset between the frequency of the incoming

communication signal and the sampling rate based on the output of the FFT circuit, and to adjust the sampling rate based on the offset.

20. The system of claim 18, wherein the local phase signals and the series of samples are digital numbers.

21. The system of claim 18, further comprising a decimator adapted to decimate said combination signal before said combination signal is received by said FFT circuit.

09768728.012401